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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,200	LAVIE ET AL.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Final Office Action in response to Amendment filed 11/24/2004.

Claims 1-21 are pending and are hereby under examination.

Objection to the Claims, because of minor informalities, is hereby withdrawn, in response to corrections made by the Amendment.

Claim Rejections under 35 U.S.C. 112, second paragraph, is hereby withdrawn, in response to corrections made by the Amendment.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chung et al. (US Patent No. 6,446,230, issued: September 3, 2002, filed: September 14, 1998).

Regarding independent Claims 1, 8, 15, Chung discloses a method and apparatus for testing integrated circuit devices (ICs) according to (IEEE) standard 1149.1, comprising:

Transmitting an external event trigger signal, (b_capture, FIG. 6A) from the compliance enabler (504) to a scan module (scan cell, 502-1) to begin a scan operation in the IC device 500A, (FIG. 5A). In the first preferred embodiment, scan cell (502, FIG. 5A) is shown in FIG. 6A as scan cell 601, which receives one signal or a combination of signals including external event trigger (b_capture) signal.

Transmitting a synchronous scan command signal, such as (sys_clk) on line 6003, to a device core (internal scan cell, 612) located inside core logic 304 of the DUT IC device 500A, where the (sys_clk) is received from the functional system clock signal, TCK of enabler 504, which clocks flip-flop 610 during boundary scan testing and synchronizes its internal TAP controller 702 (FIG. 7A) with TAP controller 306.

When the synchronous scan command (sys_clk) signal is received by the device core internal scan cell (612) of core logic 304, the holding values stored in flip-flop 610 remain unchanged until the (sys_clk) signal clocks the flip-flop.

Transmitting the values (i_sdo) of the output of flip-flop (610) on line 6023 to external test equipment (conventional ATE) through TAP controller (306, FIG. 5A), when the synchronous scan command signal (sys_clk) is received.

Regarding Claims 2, 9, 16, Chung discloses an IEEE standard 1149.1 Test Access Port (TAP) controller 306, for connecting the external test equipment to the external event trigger signal and a scan chain signal. FIG. 7B shows the scan signals

(TDI, TRST, TMS, TCK, and TDO) embedded in a baseboard (DUT 804), which includes for illustrative purposes, three chips (804-2, 4, 6) and boundary-test connector 8048, where the chips correspond to device IC device 500A, in FIG. 5A.

Regarding Claims 3, 10, 17, Chung discloses transmitting (i_sdo) values using serial (sys_clk) to shift the values from flip-flop (610) to the external test equipment (conventional ATE) via scan cells IEEE standard 1149.1 TAP controller 306, FIG. 5A.

Regarding Claims 4, 11, 18, Chung discloses receiving the values contained in the plurality of flip-flops (610) serially by the external test equipment (conventional ATE) via TAP controller 306, storing the values contained in the plurality of flip-flops in a memory system inherently located in the external test equipment, and reporting to a user through a display unit the values contained in the plurality of flip-flops.

Regarding Claims 5, 12, 19, Chung discloses synchronizing the plurality of flip-flops 610 in the device core logic 304 using a scan clock signal (sys_clk) received from the functional system clock signal, TCK of enabler 504, which clocks flip-flop 610 during boundary scan testing and synchronizes its internal TAP controller 702 (FIG. 7A) with TAP controller 306.

Regarding Claims 6, 13, 20, Chung discloses Scan TCK signal, which is an external clock, controls the transmission timing of the values (i_sdo) of the plurality of flip-flops being serially transmitted by the clock to the external test equipment.

Regarding Claims 7, 14, 21, Chung discloses IC device 500A, (FIG. 5A), comprising a communications interface such as IEEE standard 1149.1 Test Access Port (TAP) controller 306.

Response to Arguments

Applicant's arguments filed 11/24/2004 have been fully considered but they are not persuasive. Claims 1-21 are still rejected under 35 U.S.C. 102(e) as being anticipated by Chung et al. (US Patent No. 6,446,230), as set forth in the present Office Action.

In response to Applicant's argument that Chung et al. (US Patent No. 6,446,230) is not prior art to the present application, the Applicant must submit an affidavit under 37 CFR 1.131 to overcome the claim rejections under 35 U.S.C. 102(e) as being anticipated by the Chung reference. Since the Applicant has not done so, the rejection is still proper.

In reference to independent claims 1 and 8 rejected under 35 U.S.C. 102(e), Applicant argues that Chung fails to disclose the function, "holding values contained in the plurality of flip-flops in the device core unchanged when the synchronous scan command signal is received by the device core".

In response to Applicant's argument, the Office Action, above, describes with respect to Figure 6A, transmitting a synchronous clock (sys_clk) on line 6003, to (internal scan cell, 612) located inside core logic 304, which clocks flip-flop 610 and stores initially the value on line 6021 at the D-input. The initial stored value appearing at the output of flip-flop 610 remains unchanged or frozen regardless of the state of (sys_clk), unless the value on line 6021 at the D-input changes state. For example if the initial value is logic level "0", the output will remain logic level "0" regardless of the

number of (sys_clk) clock pulses, unless the D-input changes state to logic level "1", which is a well known operation for a D-type flip-flop fro those skilled in the art.

In response to Applicant's argument, with respect to independent claim 8, clearly Chung discloses transmitting the values (i_sdo) form the output of flip-flop (610) corresponding to scan cell 601 which is implemented with a plurality of flip-flop in series as a boundary scan chain in accordance with IEEE standard 1149.1, as shown in Figure 5. The boundary scan chain communicates with the external test equipment (conventional ATE) through TAP controller (306, Figure 5A), when the synchronous scan command signal (sys_clk) is received.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Date: 1 March 2005
Office Action: Final Rejection

By: 

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GUY J. LAMARRE
PRIMARY EXAMINER